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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 7

Application Number: 09/340,074
Filing Date: June 25, 1999
Appellant(s): Arimilli et al

Brian F. Russell
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed January 15, 2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that for purpose of this Appeal, claims 1-7, 10-18 and 21-27 stand or fall together as a single group.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

5,737,751 Patel et al 4-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7, 10-18 and 21-27 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Patel et al (USPN 5,737,751).

As to claim 1, Patel discloses a method of operating a multi-level cache of a computer system (see column 2 lines 20-24), comprising the steps of: monitoring cache activity of an upper level cache and a lower level cache both associated with a processor of the computer system (i.e., monitoring the cache activity of L1 cache 14 and L2 cache 20 which are both associated with the processor 12 of the computer system 10; see figure 2 and column 5 lines 42-63); the monitoring including monitoring cache hits in the upper level cache (see figure 3 and column 3 lines 5-10); issuing a request from the processor to load a value, wherein the request misses the upper level cache and the lower level cache (i.e., the processor 12 issues memory request to the multi-level storage system which comprises L1 cache 14 and L2 cache 20, wherein the request misses both the L1 cache 14 and L2 cache 20; see column 5 lines 42-44, 59-63); and selecting a victim cache block in the lower level cache for receiving the requested value based at least in part on the prior cache activity of the upper level cache (i.e., the reload queue of the L2 cache is selected for receiving the requested value for sending to both L1 cache and L2 cache based on the prior cache misses activity of L1 cache; see column 3 lines 5-10). By this rationale, claim 1 is rejected.

As to claim 2, Patel discloses that the victim cache block is further selected based in part on the cache activity of the lower level cache (i.e., the reload queue of L2 cache is selected not only based on the cache miss activity of L1 cache, but also based on the cache miss activity of the lower level L2 cache; see column 3 lines 5-10). By this rationale, claim 2 is rejected.

As to claim 3, Patel discloses that the selecting step takes place out of a critical path of execution of a core of the processor (i.e., the selecting steps are taking place from the execution unit of processor 12; see column 4 lines 40-50). By this rationale, claim 3 is rejected.

As to claim 4, Patel discloses that the issuing step issues a request to load operand data (i.e., the CPU requests a block of data or instructions from cache; see column 1 lines 66-67). By this rationale, claim 4 is rejected.

As to claim 5, Patel discloses that the selecting step includes the step of identifying a less recently used cache block in the lower level cache (see column 3 lines 27-30).

As to claim 6, Patel discloses the steps of: returning the requested value to the processor, determining that it would be efficient to currently load into the upper level cache a cache line which includes the requested value and in response to the determining step, loading the cache line into the upper level cache (i.e., when the processor issues a store request for data, the requested data is loaded only to the upper level L1 cache and the processor; see column 4 lines 4-7). By this rationale, claim 6 is rejected.

As to claim 7, Patel discloses that the monitoring step monitors cache misses of the upper level and lower level cache and the selecting step selects the victim cache block based at least in

part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale, claim 7 is rejected.

As to claim 10, Patel discloses the steps of selecting a victim cache block in the upper level cache for receiving the requested value based at least in part on the cache activity of the lower level cache (i.e., when the processor issues a store request after detecting the memory request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper level L1 cache only; see column 4 lines 4-7). By this rationale, claim 10 is rejected.

As to claims 11 and 22, Patel discloses a computer system (i.e., the computer system 10 depicted in figure 2; see column 4 lines 37-38), comprising: a system memory device (i.e., the main memory 22 in figure 2; see column 5 lines 8-11); means for processing program instructions (i.e., the processor 12; see column 4 lines 40-50); means connected to the processing means for caching values stored in the system memory device, the caching means having at least an upper level cache and a lower level cache both associated with the processing means (i.e., the upper level L1 cache 14 and lower level L2 cache; see figure 2 and column 4 lines 51-67); means for monitoring cache activity of the upper level cache and lower level cache (see column 5 lines 59-63) including cache hits in the upper level cache (see column 3 lines 5-10); and means for selecting a victim cache block in the lower level cache for receiving a value specified in a load request issued by the processing means, wherein the load request missed the upper level cache and the lower level cache, based at least in part on the cache activity of the upper level cache (see column 3 lines 5-10). By this rationale, claims 11 and 22 are rejected.

As to claim 12, Patel discloses that the selecting means is located out of a critical path of execution of a core of the processing means (i.e., the execution unit of processor 12; see column 4 lines 40-50). By this rationale, claim 12 is rejected.

As to claims 13 and 23, Patel discloses that the upper level cache is an operand data cache (i.e., the L1 Icache and L1 Dcache; see column 2 lines 34-35). By this rationale, claims 13 and 23 are rejected.

As to claim 14, Patel discloses that the selecting means identifies a less recently used cache block in the upper level cache (see column 3 lines 27-34). By this rationale, claim 14 is rejected.

As to claim 15, Patel discloses that the upper level cache is an L1 cache and the lower level cache is an L2 cache (see figure 2 and column 4 lines 51-67). By this rationale, claim 15 is rejected.

As to claims 16 and 24, Patel discloses that the upper level cache is a store-through cache (i.e., any data stored in the upper level L1 cache is also stored in the L2 cache; see column 2 lines 36-45). By this rationale, claims 16 and 24 are rejected.

As to claims 17 and 25, Patel discloses the means for returning the requested value to the processing means in response to the load request missing the upper level cache and the means for loading a cache line which includes the requested value into the upper level cache in response to a determination that it would be efficient to currently load the cache line into the upper level cache (i.e., when the processor issues a store request for data, the requested data is loaded only to the

upper level L1 cache and the processor; see column 4 lines 4-7). By this rationale, claims 17 and 25 are rejected.

As to claims 18 and 26, Patel discloses that the monitoring means monitors cache misses of the lower level cache and the selecting means selects the victim cache block based at least in part on the cache misses of the lower level cache (see column 5 lines 59-63). By this rationale, claims 18 and 26 are rejected.

As to claims 21 and 27, Patel discloses the means for selecting a victim cache block in the upper level cache for receiving the requested value based at least in part on the cache activity of the lower level cache (i.e., when the processor issues a store request after detecting the memory request misses of both L1 cache and L2 cache, the retrieved cache lines are stored in the upper level L1 cache only; see column 4 lines 4-7). By this rationale, claims 21 and 27 are rejected.

(11) Response to Argument

1. In the brief, Appellants argued that Patel clearly fails to mention selection of the victim cache block and certainly does not teach, suggest or motivate selecting a victim cache block in the lower level cache for receiving the requested value based at least in part on cache hits in the upper level cache as claimed.

In response to Appellants' argument 1, Patel clearly teaches the selection of a victim cache block by teaching that if there is a memory access miss occurring in accessing on-chip level-one cache (L1), the level-two cache (L2) is then accessed for the requested data (see column 6 lines 59-67 and column 7 lines 1-13). Also, Patel discloses the selection of a victim

in a lower level (L2) cache utilizing cache hit information for an upper level cache (L1) by teaching a weak inclusion concept which states that the L1 cache contains a subset of the block of memory in the L2 cache but that changes to the L1 cache are updated in the L2 cache periodically using a write-back operation (see column 2 lines 42-45).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

F.T.

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March 13, 2002

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